

## **Amendments to Claims**

This listing of claims will replace all prior versions and listings of claims in the application:

### **Listing of Claims**

1. (previously presented) An integrated circuit, comprising:

an execution engine clocked at a first clock rate;

a memory controller clocked at a second clock rate less than the first clock rate;

a plurality of pins adapted to transfer data to and from the memory controller on both the rising and falling edges of a second clock signal transitioning at the second clock rate; and

a multiplexer coupled to receive a first clock signal that transitions at the first clock rate and the second clock that transitions at the second clock rate, wherein the multiplexer is coupled to send the second clock signal to the memory controller during times when the memory controller receives a power supply voltage.

2. - 3. (canceled)

4. (original) The integrated circuit as recited in claim 1, wherein the memory controller is adapted to produce both a true and complementary said second clock signal on a pair of output pins of the integrated circuit.

5. (original) The integrated circuit as recited in claim 1, wherein the plurality of pins are adapted to transfer data faster than the first clock rate.

6. (currently amended) The integrated circuit as recited in claim 1, further comprising:

a configuration register adapted to store a logic value; and

~~a multiplexer; and~~

a latch having an input coupled to the configuration register and an output coupled to a select input of the multiplexer for selecting the second clock signal in lieu of a first clock signal depending on a logic voltage value stored within the configuration register.

7. (original) The integrated circuit as recited in claim 1, wherein the memory controller is coupled to receive a power supply voltage less than 2.5 volts.

8. (original) The integrated circuit as recited in claim 1, wherein the integrated circuit comprises a plurality of bonding pads wire bonded to corresponding leads emanating from the integrated circuit.

9. - 24. (canceled)